REMARKS

I. Introduction

In response to the pending Office Action, Applicants have cancelled claim 2, without prejudice, and amended claims 1 and 3-10 so as to more specifically claim the subject matter of the present invention, and to address the rejections thereof set forth under 35 U.S.C. § 112, second paragraph. In addition, new claims 11-12 have been added. New claims 11 and 12 substantial track original claims 1 and 2, respectively. No new matter has been added.

It is noted that claims 4-6 and 10 have been rewritten into independent format including all of the limitations of the underlying base claims. As such, as claims 4-8 and 10 were only objected to, and that objection has been addressed via amendment, it is respectfully submitted that claims 4-8 and 10 are now in condition for allowance.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art.

II. The Rejection Of Claims 1-3 And 9 Under 35 U.S.C. § 103

Claims 1-3 and 9 were rejected under 35 U.S.C. § 103 as being unpatentable over USP No. 5,471,409 to Tani. Applicants respectfully submit that, as amended, claims 1 and 9 are clearly patentable over Tani for at least the following reasons.

Referring to Fig. 2, for example, the present invention relates to a verification method (and a circuit for performing the same) wherein: (1) the simulating operation is performed with respect to time at a plurality of specific times, which are incrementally increasing, (2) the results of the simulating step are stored in memory after each simulating operation, and (3) the verification process is performed after each simulating operation (i.e., at each of the plurality of specific times).

Thus, in accordance with the present invention, after each of a plurality of simulating operation steps of the semiconductor circuit, which are performed with respect to time, the results of the simulating operation are stored, and it is determined whether or not the circuit elements satisfy voltage and/or current specifications.

As a result of the foregoing process, the method of the present invention enables high-speed operation of the verification step, which determines whether or not the circuit elements being verified satisfy the loaded condition requirements. Moreover, the present invention eliminates the requirement of having sufficient memory (e.g., a hard disk drive) for storing the results/data of the entire operation simulation, which is required when performing the verifying step subsequent to the simulation operation step. Thus, the present invention allows for the foregoing testing utilizing a relatively inexpensive computation system.

Turning to the cited prior art, it is again respectfully submitted that Tani fails to disclose or suggest the method or system in which the simulating operation step and the condition verifying step are performed as recited by the pending claims. Specifically, in contrast to the present invention, it appears Tani is practicing the prior art disclosed in the background section of the Applicants' specification, wherein the circuit simulation is performed first and all results are stored in a large-capacity memory device, such as a hard disk, which operates at a low speed, and thereafter (i.e., once the circuit simulation is complete) the loaded condition verification task is performed using the data stored in the large-capacity memory device.

For example, referring to Fig. 12 of Tani, this flowchart indicates that the verification step is performed as a single step after the entire simulation process is completed. Indeed, none of the various flowcharts of Tani appear to disclose that multiple simulating operations are

performed with respect to time, or that a verification step is performed after each simulating operation.

As such, it is respectfully submitted that Tani does not disclose performing multiple simulating operations at a plurality of distinct times, which are incrementally increasing, and verifying the circuit elements satisfy the predefined requirements after each simulating operation.

Accordingly, as each and every claim limitation must be disclosed or suggested by the prior art reference in order to establish a *prima facie* case of obviousness (*see*, M.P.E.P. § 2143.03), and Tani fails to do so for at least the foregoing reasons, it is respectfully submitted that claims 1 and 9, as amended, are patentable over Tani.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as all pending independent claims are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

IV. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 12/18/03

By: _____
Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W. , Suite 1200
Washington, D.C. 20005-3096
Telephone: 202-756-8000 MEF:men
Facsimile: 202-756-8087